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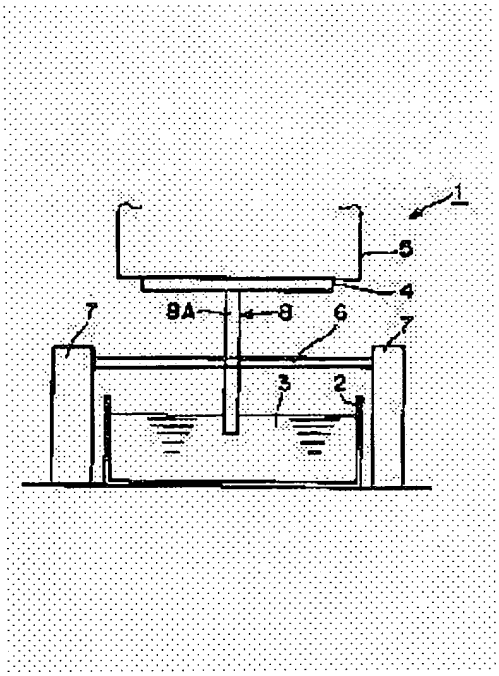
(54) MANUFACTURE AND EQUIPMENT FOR MANUFACTURING SOI MULTILAYERED SEMICONDUCTOR SUBSTRATE

(57)Abstract:
PURPOSE: To reduce irregularity of a SOI film thickness, obtain uniform SOI film thickness, eliminate possibility of over-polish, and reduce working cost.
CONSTITUTION: The title manufacturing method of an SOI multilayered semiconductor substrate 4 constists of the following; a process for measuring the SOI film thickness distribution on the whole surface of the substrate 4, and a process for locally etching the SOI film of the thick portion of the substrate 4, on the basis of the measured value, by using a holding member 8A which holds etching solution 3 for etching silicon and comes into contact with the silicon surface of the substrate 4 while rotating. The title manufacturing equipment is provided with the following; a fixing part 6 for fixing the substrate 4, the holding member 8A which holds the etching solution for etching silicon and comes into contact with the silicon surface of the fixed substrate 4 while rotating, a rotary holding part which moves while rotating the holding member 8A, and an etching solution supplying part 2 for feeding the etching solution to the holding member 8A.



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CLAIMS

[Claim(s)]
[Claim 1] The process which is the manufacture approach of the SOI laminating semi-conductor substrate which a dielectric is made to intervene, pastes up the semiconductor wafer of at least two sheets, and forms SOI thickness in homogeneity, and measures the SOI thickness distribution covering the whole surface of said SOI laminating semi-conductor substrate, By the maintenance material which contacts while holding the etching reagent which etches silicon and rotating to the silicon side of said fixed SOI laminating semi-conductor substrate The manufacture approach of the SOI laminating semi-conductor substrate characterized by having the process which etches locally the SOI film of a part with said thick SOI laminating semi-conductor substrate based on said measurement value.
[Claim 2] The fixed part which is the manufacturing installation of the SOI laminating semi-conductor substrate which a dielectric is made to intervene, pastes up the semiconductor wafer of at least two sheets, and forms SOI thickness in homogeneity, and fixes said SOI laminating semi-conductor substrate, The maintenance material which contacts while holding the etching reagent which etches silicon and rotating to the silicon side of said fixed SOI laminating semi-conductor substrate, The manufacturing installation of the SOI laminating semi-conductor substrate characterized by having the rotation supporter which moves the maintenance material concerned in the direction of a three dimension while rotating this maintenance material, and the etching-reagent feed zone which supplies said etching reagent to said maintenance material.

[Claim 3] The manufacturing installation of the SOI laminating semi-conductor substrate according to claim 2 which is the etching tub to which said etching-reagent feed zone contained the etching reagent with which said rotating maintenance material is immersed.
[Claim 4] The manufacturing installation of the SOI laminating semi-conductor substrate according to claim 2 said whose etching-reagent feed zone is the spray which blows an etching reagent upon said rotating maintenance material.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention makes a dielectric layer intervene between the 1st silicon wafer and the 2nd silicon wafer, and relates to the manufacture approach of the SOI laminating semi-conductor substrate pasted up and formed, and its manufacturing installation.
[0002]
[Description of the Prior Art] In the former, a dielectric layer is made to intervene between the 1st silicon wafer and the 2nd silicon wafer, and the SOI (Silicon on Insulator) laminating semi-conductor substrate pasted up and formed is known.
[0003] The above-mentioned conventional SOI laminating semi-conductor substrate 4 is formed in sequence as shown for example, in drawing 4 (a) - (f). Drawing 4 (a) - (f) is the sectional view showing the order of a production process.
[0004] First, as shown in drawing 4 (a), the front face of the 1st silicon wafer 11 by which mirror polishing was carried out is oxidized, the oxide film 12 whose thickness is about 0.5 micrometers is formed, and defecation processing on the front face of adhesion of the both sides of the 1st silicon wafer 11 and the 2nd silicon wafer 13 is performed.
[0005] Next, as shown in drawing 4 (b), stick the 1st silicon wafer 11 and the 2nd silicon wafer 13 at a room temperature, heat-treat above the temperature C of 800 degrees, an oxide film (dielectric layer) 12 is made to intervene among both silicon wafers 11 and 13, and it pastes up.
[0006] Furthermore, as shown in drawing 4 (c), the slot 14 of 17.5mm angle is formed in the 1st silicon wafer 11 in the shape of a grid along a dicing line in the depth which leaves about 10 micrometers of the 1st silicon wafers 11 with the diamond blade of about 1mm of edge thickness.
[0007] Next, base 14a of the above-mentioned slot 14 is etched by KOH until it reaches the oxide film 12 which exists in the middle of the 1st silicon wafer 11 and the 2nd silicon wafer 13, as shown in drawing 4 (d).
[0008] And as shown in drawing 4 (e), the thin film 15 of the quality of the material with a polish rate slower than a silicon wafer, for example, an oxide film, is formed in the above-mentioned groove bottom side 14a about 0.2 under the same conditions. Finally, as shown in drawing 4 (f), the SOI laminating semi-conductor substrate 4 is manufactured by making the front face of the 1st silicon wafer 11 in agreement with the top face of the oxide-film layer 15 formed in the above-mentioned groove bottom side 14a, and forming the active-region layer 16 by grinding polish.
[0009]
[Problem(s) to be Solved by the Invention] However, in the SOI laminating semi-conductor substrate manufactured by the above-mentioned conventional manufacture approach, although it was possible to have adjusted the thickness (thickness) of an active-region layer with the thickness of an oxide film, when the SOI thickness equalized more was required, it was difficult [it] for there to be a problem by which an exaggerated polish is carried out and to fill the above-mentioned demand. Moreover, according to this approach, although the dirty stopping method is learned as an equalization technique of SOI thickness, since processing by various kinds of down stream processing is required, there is a problem on which processing

cost increases. Furthermore, although the partial plasma dirty method etc. is proposed, there is a problem on which processing cost increases also in this approach.
[0010] Then, this invention has little variation in SOI thickness, does not have worries about an exaggerated polish and aims at offering the manufacture approach of a SOI laminating semi-conductor substrate and equipment which can reduce processing cost while it can obtain the SOI thickness equalized more.
[0011]
[Means for Solving the Problem] The manufacture approach of the SOI laminating semi-conductor substrate concerning this invention The process which is the manufacture approach of the SOI laminating semi-conductor substrate which a dielectric is made to intervene, pastes up the semiconductor wafer of at least two sheets, and forms SOI thickness in homogeneity, and measures the SOI thickness distribution covering the whole surface of said SOI laminating semi-conductor substrate, By the maintenance material which contacts while holding the etching reagent which etches silicon and rotating to the silicon side of said fixed SOI laminating semi-conductor substrate It considers as the configuration equipped with the process which etches locally the SOI film of a part with said thick SOI laminating semi-conductor substrate based on said measurement value.
[0012] Moreover, the manufacturing installation of the SOI laminating semi-conductor substrate concerning this invention The fixed part which is the manufacturing installation of the SOI laminating semi-conductor substrate which a dielectric is made to intervene, pastes up the semiconductor wafer of at least two sheets, and forms SOI thickness in homogeneity, and fixes said SOI laminating semi-conductor substrate, The maintenance material which contacts while holding the etching reagent which etches silicon and rotating to the silicon side of said fixed SOI laminating semi-conductor substrate, It considers as the configuration equipped with the rotation supporter which moves the maintenance material concerned in the direction of a three dimension while rotating this maintenance material, and the etching-reagent feed zone which supplies said etching reagent to said maintenance material. Furthermore, said etching-reagent feed zone is constituted by the etching tub which contained the etching reagent with which said rotating maintenance material is immersed, and the spray which blows an etching reagent upon said rotating maintenance material.
[0013]
[Function] Therefore, since according to this invention holding the etch rate by maintenance material uniformly can control while etching the thick part of SOI thickness alternatively based on the measurement value of SOI thickness, it is few and etching control of uniform thickness is attained, the variation in SOI thickness can obtain the SOI thickness equalized more, and the creation of MOS of high quality of it is attained. Furthermore, there are no worries about an exaggerated polish like before, and processing cost can be reduced.
[0014]
[Example] Below, one example of this invention is explained based on a drawing. Drawing 1 and drawing 2 are the front views and side elevations of a SOI laminating semi-conductor substrate manufacturing installation concerning this example.
[0015] The vacuum chuck (fixed part) 5 by which the SOI laminating semi-conductor substrate manufacturing installation 1 of this example fixes the SOI laminating semi-conductor substrate 4 above the etching tub (etching-reagent feed zone) 2 by suction as shown in drawing 1 and drawing 2 is formed. The upper part carries out opening of the above-mentioned etching tub 2, and the etching reagent 3 which consists of an etching reagent 3, for example, the mixed liquor of HF and HNO3, or mixed liquor of HF and H2O2 is contained inside.
[0016] Moreover, between the above-mentioned etching tub 2 and a vacuum chuck 5, a revolving shaft 6 is arranged horizontally, the drive supporter 7 moved to X, Y, and a Z direction in three dimension is arranged in the both-ends side of this revolving shaft 6, supporting the both ends of a revolving shaft 6 to revolve, while rotating this revolving shaft 6, and it connects with the controller which these drive supporters 7 do not illustrate electrically.
[0017] Furthermore, to the above-mentioned revolving shaft 6, it has fixed so that a revolving shaft 6 and the body of revolution 8 by which maintenance material 8A was stuck on the peripheral surface may cross at right angles. This body of revolution 8 is formed in the discoid whose thickness dimension is 1-2mm, and it is

formed in the same width of face, and maintenance material 8A is also formed in the path to which the bottom can be flooded with the etching reagent 3 in the above-mentioned etching tub 2 while the maintenance material 8 can contact the front face of the SOI laminating semi-conductor substrate 4 fixed to the above-mentioned vacuum chuck 5 in the upper part. Moreover, this maintenance material 8A consists of etching-proof nature using the quality of the material which does not give a blemish to the silicon side of the SOI laminating semi-conductor substrate 4, for example, a cross etc., makes the etching reagent 3 in the etching tub 2 permeate, and is held inside.

[0018] And if body of revolution 8 and maintenance material 8A rotate in connection with a revolving shaft 6, the etching reagent 3 in the etching tub 2 adheres to the interior of maintenance material 8A, and it has the structure where the silicon side of the SOI laminating semi-conductor substrate 4 fixed to the vacuum chuck 5 with this adhering etching reagent 3 is etched.

[0019] Next, the case where equalization processing of the silicon side of the SOI laminating semi-conductor substrate 4 is carried out using the manufacturing installation 1 of the above-mentioned configuration is explained.

[0020] First, in order to manufacture the SOI laminating semi-conductor substrate 4, as shown in drawing 3 (a), the front face where mirror polishing of the 1st silicon wafer 11 was carried out is oxidized, and the oxide film 12 with a thickness of about 0.5 micrometers is formed. And defecation processing of the front face of the both sides of the 1st silicon wafer 11 and the 2nd silicon wafer 13 is performed.

[0021] Next, as shown in drawing 3 (b), the 1st silicon wafer 11 and the 2nd silicon wafer 13 are stuck at a room temperature through an oxide film 12, and it heat-treats, the oxide-film ambient atmosphere, for example, the steam ambient atmosphere, beyond the temperature C of 800 degrees, and an oxide film 12 is made to intervene and the 1st silicon wafer 11 and the 2nd silicon wafer 13 are pasted up.

[0022] Next, the top face of the 1st silicon wafer 11 is thin-film-ized by grinding polish, and it considers as the SOI laminating semi-conductor substrate with which SOI thickness has 1-5 micrometers.

[0023] Furthermore, as shown in drawing 1 , it fixes by the vacuum chuck 5, the SOI laminating semi-conductor substrate 4 by which the laminating was carried out is set, and the SOI thickness covering the whole surface of this SOI laminating semi-conductor substrate 4 is measured.

[0024] And based on the thickness measurement value of the above-mentioned SOI laminating semi-conductor substrate 4, maintenance material 8A is moved to the thick part of thickness, rotating a revolving shaft 6 with the drive supporter 7, and rotating body of revolution 8 and maintenance material 8A in connection with this, as shown in drawing 3 (c). In this case, the above-mentioned drive supporter 7 is controlled by the controller based on the above-mentioned measurement value.

[0025] Then, move maintenance material 8A upwards with the drive supporter 7, the front face of the SOI laminating semi-conductor substrate 4 which is going to etch the upper part of maintenance material 8A is made to contact, a silicon side is etched by the etching time based on the amount of etching, or the etch rate of an etching reagent 3, and as shown in drawing 2 (d), the SOI laminating semi-conductor substrate 4 with the more uniform SOI thickness of the active-region layer 16 is obtained.

[0026] And it can be made a mirror plane when the mirror plane of the active-region layer front face of the SOI laminating semi-conductor substrate 4 grinds to a rough ******** case after the completion of etching following on etching.

[0027] In addition, you may make it move even if it moves maintenance material to a degree in this case, making it predetermined SOI thickness for every place, and so that it may etch gradually, scanning the whole surface covering two or more thick parts. Furthermore, as an engine speed of maintenance material, it is set up so that an etching reagent may not disperse around maintenance material.

[0028] Moreover, in the above-mentioned example, although width of face of maintenance material was set to 1-2mm, in being thick, when it covers the whole field, and the SOI thickness of a SOI laminating semi-conductor substrate etches to some extent using the big maintenance material of width of face previously and etches, using the maintenance material of the above-mentioned 1-2mm width of face as the last finishing, efficient etching processing can be performed. Moreover, it chooses with the equalization level of SOI thickness also as an etching reagent, and in equalizing more, he is trying to use an etching reagent with a small etch rate.

[0029] Furthermore, as an etching-reagent feed zone which supplies an etching reagent to the above-mentioned maintenance material, the spray which blows not only an etching tub but an etching reagent upon maintenance material can also be used.
[0030] Therefore, in this example, in order to etch the thick part of SOI thickness alternatively based on the measurement value of SOI thickness, the SOI laminating semi-conductor substrate of uniform SOI thickness can be obtained. Furthermore, since an etch rate can be uniformly held in order to make the etching reagent held at the maintenance material which etches SOI thickness always refresh, it becomes controllable [more uniform thickness].
[0031]
[Effect of the Invention] Since the etch rate by maintenance material can be uniformly held according to this invention while etching the thick part of SOI thickness alternatively based on the measurement value of SOI thickness as explained above, variation has little SOI thickness, etching control of uniform thickness is attained, the SOI thickness equalized more can be obtained and creation of MOS of high quality is attained. Furthermore, there are no worries about an exaggerated polish like before, and processing cost can be reduced. And according to the result which this invention person examined, the uniform SOI laminating semi-conductor substrate of 0.1-micrometer SOI thickness was able to be obtained.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the front view showing the manufacturing installation of the SOI laminating semi-conductor substrate concerning this invention.
[Drawing 2] It is the side elevation showing the manufacturing installation of a SOI laminating semi-conductor substrate.
[Drawing 3] (a) - (d) is the sectional view showing the production process of the SOI laminating semi-conductor substrate concerning this invention.
[Drawing 4] (a) - (e) is the sectional view showing the production process of the conventional SOI laminating semi-conductor substrate.
[Description of Notations]
1 Manufacturing Installation
2 Etching-Reagent Feed Zone (Etching Tub)
3 Etching Reagent
4 SOI Laminating Semi-conductor Substrate
6 Fixed Part
7 Rotation Mechanical Component
8A Maintenance material
11 1st Silicon Wafer
12 Dielectric (Oxide Film)
13 2nd Silicon Wafer

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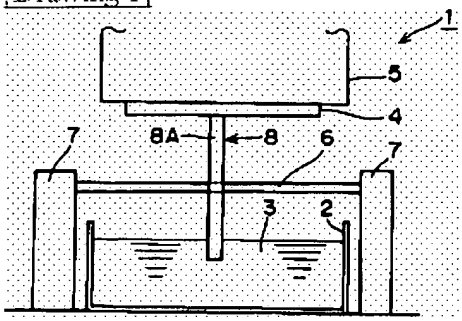
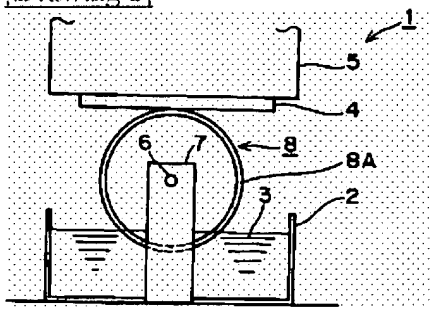
DRAWINGS

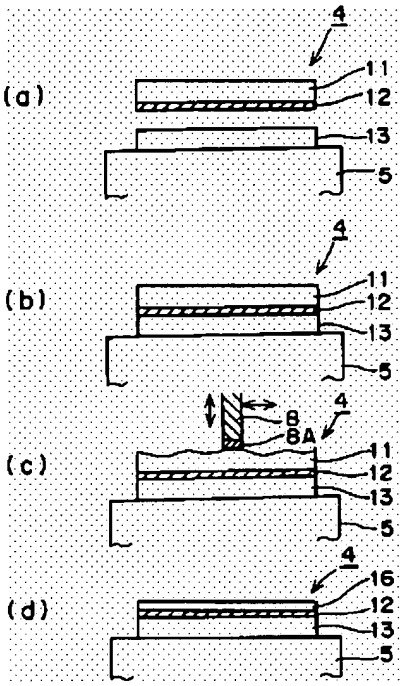
[Drawing 1]



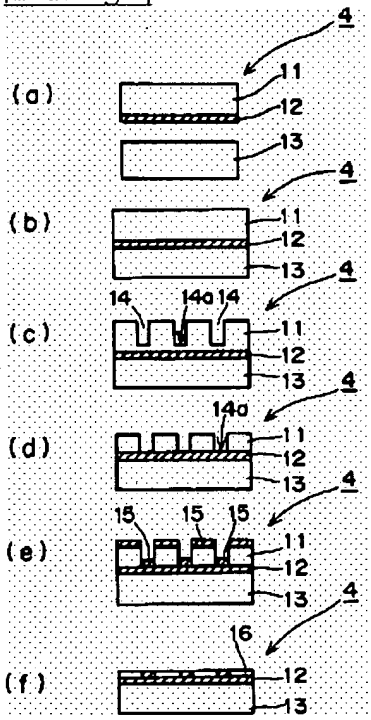
[Drawing 2]



[Drawing 3]



[Drawing 4]



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